Amendments to the Claims

Please cancel claims 7, 8, 23, 24, 32-35, 37, 52, 55-60, 62, 76, 78, 82-84, 86, 88, 95-96, 104-105 and 114, add new claims 117-140, and amend the remaining claims as shown below.

Listing of Claims

1. (Currently Amended) A method for adaptively updating coefficients in a filter for processing data, comprising the steps of:

   a) receiving a data sequence in the filter and processing the data sequence in accordance with the coefficients in the filter to produce a processed data sequence;

   b) filtering the data sequence with a first set of filter characteristics to generate a filtered data term for the coefficients;

   c) ~~generating a filtered error term for the coefficients from at least~~ filtering the processed data sequence using a second set of filter characteristics, said second set of filter characteristics being structurally and/or functionally identical to said first set of filter characteristics; ~~and~~

   d) generating a filtered ideal processed data sequence from the processed data sequence using a third set of filter characteristics, said third set of filter characteristics comprising a subset of filter characteristics structurally and/or functionally identical to said first filter characteristics;

   e) generating a filtered error term for the coefficients from the filtered processed data sequence and the filtered ideal processed data sequence; and

   f) updating the coefficients in the filter with each of said filtered data term and said filtered error term.

2. (Currently Amended) The method of Claim 1, wherein ~~said generating step c)~~ filtering the processed data sequence comprises convolving the processed data sequence with said second set of filter characteristics to generate [[a]] the filtered processed data sequence.

3. (Currently Amended) The method of Claim 2, wherein ~~said~~ generating ~~step c) further~~ the filtered error term comprises determining a difference between the filtered processed data sequence and ~~an ideal~~ the filtered ideal processed data sequence ~~to produce said filtered error term~~.

4. (Currently Amended) The method of Claim 3, further comprising (i) detecting a sequence of said processed data sequence, and (ii) convolving said sequence-detected processed data sequence with [[a]] said third set of filter characteristics to generate said ~~ideal~~ filtered ideal processed data sequence.

5. (Currently Amended) The method of Claim [[4]]1, wherein said first set of filter characteristics is identical to said second set of filter characteristics.

6. (Currently Amended) The method of Claim [[4]]1, wherein at least part of said third set of filter characteristics ~~comprising a subset of filter characteristics structurally and/or functionally~~ is identical to said first and second sets of filter characteristics.

7. (Canceled)

8. (Canceled)

9. (Currently Amended) The method of Claim [[7]]1, ~~further comprising (i)~~ wherein generating the filtered ideal processed data sequence comprises further processing said processed data sequence with a sequence detector, and ~~(ii)~~ convolving said sequence-detected processed data sequence with [[a]] the third set of filter characteristics ~~to generate said ideal filtered processed data sequence~~.

10. (Original) The method of Claim 1, wherein each of said first and second sets of filter characteristics comprises an error filter.

11. (Original) The method of Claim 10, wherein said filtering further comprises transposing a channel response to generate at least a subset of said first set of filter characteristics.

12. (Original) The method of Claim 1, wherein said data sequence comprises a digital data signal.

13. (Currently Amended) The method of Claim [[3]]1, wherein said processing step a) comprises equalizing said data sequence, said processed data sequence comprises an equalized data signal, said filtered processed data sequence comprises a filtered equalized data signal, and said ideal filtered processed data sequence comprises an ideal filtered equalized data signal.

14. (Original) The method of Claim 1, wherein said first and second sets of filter characteristics are configured to minimize a dominant error type.

15. (Original) The method of Claim 14, wherein said dominant error type comprises a single bit error.

16. (Original) The method of Claim 15, wherein said first and second sets of filter characteristics are further configured to minimize a dibit error.

17. (Currently Amended) A computer-readable medium containing a set of instructions which, when executed by a signal processing device configured to execute computer-readable instructions, is configured to perform a method comprising:

processing a data sequence in accordance with coefficients in a filter to produce a processed data sequence;

filtering the data sequence with a first set of filter characteristics to generate a filtered data term;

~~generating a filtered error term for the coefficients from at least~~ filtering the processed data sequence using a second set of filter characteristics, said second set of filter characteristics being structurally and/or functionally identical to said first set of filter characteristics; ~~and~~

generating a filtered ideal processed data sequence from the processed data sequence using a third set of filter characteristics, said third set of filter characteristics comprising a subset of filter characteristics structurally and/or functionally identical to said first of filter characteristics;

generating a filtered error term for the coefficients from the filtered processed data sequence and the filtered ideal processed data sequence; and

updating the coefficients in the filter with each of said filtered data term and said filtered error term.

18. (Previously Presented) The computer-readable medium of Claim 17, wherein said coefficients are for an adaptive finite impulse response (FIR) algorithm.

19. (Previously Presented) The computer-readable medium of Claim 18, wherein said coefficients are derived from comprises a least-mean-squares (LMS) gradient algorithm.

20. (Previously Presented) The computer-readable medium of Claim 17, wherein said processing step a) comprises equalizing said data sequence.

21. (Currently Amended) The computer-readable medium of Claim 17, wherein ~~said~~ generating ~~step c)~~ the filtered ideal processed data sequence comprises (i) detecting a sequence of said processed data sequence, and (ii) convolving said sequence-detected, processed data sequence with said ~~second~~ third set of filter characteristics ~~to generate a filtered processed data sequence~~.

22. (Currently Amended) The computer-readable medium of Claim 21, wherein ~~said~~ generating ~~step c) further~~ said filtered error term comprises subtracting ~~an~~ the ideal filtered processed data sequence from the filtered processed data sequence ~~to generate said filtered error term~~.

23. (Canceled)

24. (Canceled)

25. (Previously Presented) The computer-readable medium of Claim 17, wherein each of said first and second sets of filter characteristics comprises an error filter.

26. (Previously Presented) The computer-readable medium of Claim 17, wherein said method further comprises minimizing a dominant error type.

27. (Previously Presented) The computer-readable medium of Claim 26, wherein said dominant error type comprises a single bit error.

28. (Previously Presented) The computer-readable medium of claim 17, wherein said set of instructions comprises object code, source code and/or binary code.

29. (Previously Presented) The computer-readable medium of claim 17, wherein said set of instructions comprises digital code configured for processing by a digital data processor.

30. (Currently Amended) A method for updating coefficients in a filter for processing data, comprising the steps of:

a) processing a data sequence in accordance with the coefficients in the filter to produce a processed data sequence;

b) filtering the data sequence to generate a filtered data term for the coefficients using a first set of filter characteristics;

c) detecting a sequence of said processed data sequence to generate an ideal processed data sequence;

d) determining a difference between the processed data sequence and the ideal processed data sequence to produce an error term;

e) ~~filtering an~~ generating a filtered error term for the coefficients ~~generated~~ from ~~at least~~ the processed data sequence error term, using at least a second set of filter characteristics structurally and/or functionally identical to said first set of filter characteristics; and

f) updating the coefficients with each of said filtered data term and said filtered error term.

31. (Currently Amended) The method of Claim 30, wherein said second set of filter characteristics is ~~structurally and functionally~~ identical to said first set of filter characteristics.

32. (Canceled)

33. (Canceled)

34. (Canceled)

35. (Canceled)

36. (Currently Amended) The method of Claim [[35]]30, wherein ~~said filtering step e)~~ generating said error term further comprises convolving the error term with a ~~second~~ filter comprising said second set of filter characteristics ~~to generate said filtered error term~~.

37. (Canceled)

38. (Original) The method of Claim 30, wherein each of said first and second sets of filter characteristics comprises an error filter.

39. (Original) The method of Claim 38, wherein said filtering further comprises transposing a channel response to generate at least a subset of said second set of filter characteristics.

40. (Original) The method of Claim 30, wherein said data sequence comprises a digital data signal.

41. (Currently Amended) The method of Claim [[33]]30, wherein said processing step a) comprises equalizing said data sequence, said processed data sequence comprises an equalized data signal, ~~said filtered processed data sequence comprises a filtered equalized data signal,~~ and said ~~ideal filtered~~ ideal processed data sequence comprises an ideal ~~filtered~~ equalized data signal.

42. (Previously Presented) The method of Claim 30, wherein said second set of filter characteristics is configured to minimize a dominant error type.

43. (Original) The method of Claim 42, wherein said dominant error type comprises a single bit error.

44. (Currently Amended) A computer-readable medium containing a set of instructions which, when executed by a signal processing device configured to execute computer-readable instructions, is configured to perform a method comprising:

processing a data sequence in accordance with coefficients in a filter to produce a processed data sequence;

filtering the data sequence to generate a filtered data term for the coefficients using a first set of filter characteristics;

detecting a sequence of said processed data sequence to generate an ideal processed data sequence;

determining a difference between the processed data sequence and the ideal processed data sequence to produce an error term;

~~filtering an~~ generating a filtered error term for the coefficients ~~generated~~ from ~~at least~~ the ~~processed data sequence~~ error term, using at least a second set of filter characteristics structurally and/or functionally identical to said first set of filter characteristics; and

updating the coefficients with each of said filtered data term and said filtered error term.

45. (Previously Presented) The computer-readable medium of Claim 44, wherein said coefficients are for an adaptive finite impulse response (FIR) algorithm.

46. (Previously Presented) The computer-readable medium of Claim 45, wherein said coefficients are derived from a least-mean-squares (LMS) gradient algorithm.

47. (Previously Presented) The computer-readable medium of claim 44, wherein said set of instructions comprises object code, source code and/or binary code.

48. (Previously Presented) The computer-readable medium of claim 44, wherein said set of instructions comprises digital code configured for processing by a digital data processor.

49. (Currently Amended) A signal processing architecture, comprising:

a) an equalizer configured to equalize and/or filter a data sequence in accordance with filter coefficients and provide an equalized data output;

b) a first filter, configured to receive said data sequence and generate a filtered data term for updating said filter coefficients; and

c) an error term circuit, configured to receive said equalized data output and provide a filtered error term for updating said filter coefficients from a filtered equalized data output and a filtered ideal equalized data output, said error term circuit comprising a second filter having filter characteristics structurally and/or functionally identical to said first filter, configured to filter said equalized data output; a signal processor configured to provide an ideal equalized data output from the equalized data output; and a third filter configured to filter said ideal equalized data output, having a subset of filter characteristics structurally and/or functionally identical to said first filter.

50. (Original) The architecture of claim 49, wherein said equalizer comprises an adaptive finite impulse response (FIR) filter.

51. (Previously Presented) The architecture of claim 50, wherein said filter coefficients are derived from a least-mean-square (LMS) algorithm.

52. (Canceled)

53. (Currently Amended) The architecture of claim [[52]]49, wherein said signal processor comprises a sequence detector ~~configured to provide a sequence detected equalized data output~~.

54. (Currently Amended) The architecture of claim [[52]]49, wherein said error term circuit further comprises a ~~third~~ target filter configured to receive an output from said signal processor and provide [[an]] said ideal equalized data output.

55. (Canceled)

56. (Canceled)

57. (Canceled)

58. (Canceled)

59. (Canceled)

60. (Canceled)

61. (Currently Amended) The architecture of claim [[52]]49, wherein said second filter receives said equalized data output and provides [[a]] said filtered equalized data output.

62. (Canceled)

63. (Currently Amended) The architecture of claim [[62]]49, wherein said third filter comprises a target filter.

64. (Currently Amended) The architecture of claim [[62]]63, wherein said ~~error term circuit further comprises a fourth~~ third filter further comprises an error filter~~configured to receive said ideal equalized data output and provide an ideal filtered equalized data output~~.

65. (Currently Amended) The architecture of claim [[64]]49, further comprising a subtractor or comparator configured to (i) receive said filtered equalized data output and said ~~ideal~~ filtered ideal equalized data output, and (ii) provide said filtered error term.

66. (Original) The architecture of claim 65, wherein said subtractor or comparator comprises said subtractor, and said subtractor is further configured to subtract one of said filtered equalized data output and said ideal filtered equalized data output from the other of said filtered equalized data output and said ideal filtered equalized data output.

67. (Original) The architecture of claim 49, wherein each of said first and second filters comprises an error filter.

68. (Original) The architecture of claim 67, wherein each of said first and second filters further comprises a matched filter.

69. (Original) The architecture of claim 67, wherein said error filter is configured to minimize one or more dominant error types.

70. (Original) The architecture of claim 69, wherein said one or more dominant error types comprise a single bit error event.

71. (Original) The architecture of claim 49, further comprising a receiver configured to receive data from a magnetic storage medium and provide said data sequence.

72. (Currently Amended) The architecture of claim 49, wherein said second filter is ~~structurally and/or functionally~~ identical to said first filter.

73. (Currently Amended) The architecture of claim [[56]]72, wherein ~~said~~ a portion of said third filter is structurally and/or functionally identical to said first and second filters.

74. (Currently Amended) A signal processing architecture, comprising:

a) means for equalizing an input data signal in accordance with filtering coefficients, configured to produce an equalized data signal;

b) first means for filtering said input data signal, configured to generate a filtered data term for updating said filtering coefficients; and

c) means for providing a filtered error term for updating said filtering coefficients~~, configured to receive~~ from said equalized data signal and an ideal equalized data signal, comprising a second means for filtering said equalized data signal, having filter characteristics structurally and/or functionally identical to said first means for filtering; a means for processing said equalized data signal, configured to provide said ideal equalized data signal; and a third means for filtering said ideal equalized data signal, having a subset of filter characteristics structurally and/or functionally identical to said first means for filtering.

75. (Original) The architecture of claim 74, wherein said means for equalizing comprises an adaptive finite impulse response (FIR) filter.

76. (Canceled)

77. (Currently Amended) The architecture of claim [[76]]74, wherein said means for processing comprises a sequence detector~~ configured to provide a sequence detected equalized data signal~~.

78. (Canceled)

79. (Currently Amended) The architecture of claim [[78]]74, wherein said third means for filtering comprises a target filter.

80. (Currently Amended) The architecture of Claim [[78]]74, said third means for filtering comprising a portion having filter characteristics structurally and/or functionally identical to said first and second filters.

81. (Original) The architecture of Claim 80, wherein said third means for filtering further comprises a target filter.

82. (Canceled)

83. (Canceled)

84. (Canceled)

85. (Currently Amended) The architecture of claim [[76]]74, wherein said second means for filtering receives said equalized data signal and provides [[a]] said filtered equalized data signal.

86. (Canceled)

87. (Currently Amended) The architecture of claim [[86]]74, wherein said means for ~~providing~~ processing said ~~filtered error term further~~ equalized data signal comprises a first means for convolving said ~~processed~~ equalized data signal with a target filter, configured to provide ~~an~~ said ideal equalized data signal.

88. (Canceled)

89. (Currently Amended) The architecture of claim [[88]]74, further comprising further comprising a means for generating said filtered error term, configured to receive said filtered equalized data signal and said ideal filtered equalized data signal.

90. (Currently Amended) The architecture of claim [[80]]89, wherein said means for generating said filtered error term comprises a subtractor, configured to subtract one of

said filtered equalized data signal and said ideal filtered equalized data signal from the other of said filtered equalized data signal and said ideal filtered equalized data signal.

91. (Original) The architecture of claim 74, wherein each of said first and second means for filtering comprises an error filter.

92. (Original) The architecture of claim 91, wherein each of said first and second means for filtering further comprises a matched filter.

93. (Original) The architecture of claim 91, wherein said error filter is configured to minimize one or more dominant error types.

94. (Original) The architecture of claim 93, wherein said one or more dominant error types comprise a single bit error event.

95. (Canceled)

96. (Canceled)

97. (Original) A system for reading magnetically recorded data, comprising:
    a) the architecture of claim 49; and
    b) at least one receiver communicatively coupled to said architecture for receiving said first data sequence.

98. (Original) The system of claim 97, wherein said equalizer comprises an adaptive finite impulse response (FIR) filter.

99. (Previously Presented) The system of claim 98, wherein said filter coefficients are derived from a least-mean-square (LMS) algorithm.

100. (Currently Amended) The system of claim 97, wherein said ~~error term circuit further~~ signal processor comprises a sequence detector configured to receive said equalized data output and provide a sequence-detected equalized data output.

101. (Currently Amended) The system of claim 100, wherein said error term circuit further comprises a ~~third~~ target filter configured to receive an output from said ~~signal processor~~ sequence detector and provide [[an]] said ideal equalized data output.

102. (Previously Presented) The system of Claim 100, said third filter comprising a portion structurally and/or functionally identical to said first and second filters.

103. (Original) The system of Claim 102, wherein said third filter further comprises a target filter.

104. (Canceled)

105. (Canceled)

106. (Original) The system of claim 101, wherein said second filter receives said equalized data output and provides a filtered equalized data output.

107. (Original) The system of claim 106, wherein said error term circuit further comprises a fourth filter configured to receive said ideal equalized data output and provide ~~an ideal~~ a filtered ideal equalized data output.

108. (Currently Amended) The system of claim 107, further comprising a subtractor or comparator configured to (i) receive said filtered equalized data output and said ~~ideal~~ filtered ideal equalized data output, and (ii) provide said filtered error term.

109. (Original) The system of claim 97, wherein each of said first and second filters comprises an error filter.

110. (Original) The system of claim 109, wherein each of said first and second filters further comprises a matched filter.

111. (Original) The system of claim 109, wherein said error filter is configured to minimize one or more dominant error types.

112. (Original) The system of claim 111, wherein said one or more dominant error types comprise a single bit error event.

113. (Currently Amended) The system of claim 97, wherein said second filter is ~~structurally and/or functionally~~ identical to said first filter.

114. (Canceled)

115. (Original) A magnetic recording system, comprising:
a) the system of Claim 97; and
b) a magnetic storage device, communicatively coupled to said system.

116. (Original) The magnetic recording system of claim 115, wherein said magnetic storage device comprises a floppy disk, a CD-ROM, a magnetic tape or a hard disk drive.

117. (New) The method of Claim 1, wherein said third set of filter characteristics comprises an error filter and a target filter.

118. (New) The method of Claim 10, wherein said third set of filter characteristics comprises said error filter and a target filter.

119. (New) The computer-readable medium of Claim 25, wherein said third set of filter characteristics comprises said error filter and a target filter.

120. (New) The architecture of claim 67, wherein said third filter comprises an error filter.

121. (New) The architecture of claim 120, wherein said third filter further comprises a target filter.

122. (New) The architecture of claim 68, wherein said third filter comprises an error filter and a matched filter.

123. (New) The architecture of claim 122, wherein said third filter further comprises a target filter.

124. (New) The architecture of claim 67, wherein said first and second filters each comprise an exact filter.

125. (New) The architecture of claim 70, wherein said first and second filters are further configured to minimize a dibit error.

126. (New) The architecture of claim 120, wherein said third filter further comprises an exact filter.

127. (New) The method of Claim 15, wherein said first and second sets of filter characteristics each comprise an exact filter.

128. (New) The computer-readable medium of Claim 27, wherein said first and second sets of filter characteristics each comprise an exact filter.

129. (New) The method of Claim 43, wherein said first and second sets of filter characteristics each comprise an exact filter.

130. (New) The computer-readable medium of Claim 44, wherein said first and second sets of filter characteristics minimize a dominant error type.

131. (New) The computer-readable medium of Claim 130, wherein said first and second sets of filter characteristics minimize a single bit error.

132. (New) The computer-readable medium of Claim 131, wherein said first and second sets of filter characteristics each comprise an exact filter.

133. (New) The computer-readable medium of Claim 130, wherein said first and second sets of filter characteristics minimize a dibit error.

134. (New) The computer-readable medium of Claim 17, wherein filtering the processed data sequence comprises convolving the processed data sequence with said second set of filter characteristics to generate the filtered processed data sequence.

135. (New) The method of Claim 43, wherein said first and second sets of filter characteristics minimize a dibit error.

136. (New) The computer-readable medium of Claim 44, wherein said second set of filter characteristics is identical to said first set of filter characteristics.

137. (New) The computer-readable medium of Claim 44, wherein generating said error term further comprises convolving the error term with said second set of filter characteristics.

138. (New) The computer-readable medium of Claim 44, wherein each of said first and second sets of filter characteristics comprises an error filter.

139. (New) The computer-readable medium of Claim 138, wherein each of said first and second sets of filter characteristics is configured to minimize a dominant error type.

140. (New) The computer-readable medium of Claim 139, wherein said dominant error type comprises a single bit error.